A New Development Framework for Multi-Core Processor based Smart-Camera Implementations

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The exponential evolution of the smart camera processing performances is directly linked to the improvements on hardware processing elements. Nowadays, high processing performances can be reached considering hardware targets which enables a high level of task parallelism to be implemented. Highly regular tasks are good candidate for a reconfigurable logic implementation and less regular parts of the algorithm could be described on the processor. Meanwhile the prototyping time is related to the selected target and the associated development methodology. The implementation on reconfigurable logic is highly efficient in exploiting the intrinsic task parallelism nevertheless can be time consuming using traditional methodology (i.e. Hardware Language Description). Several approaches can be considered to decrease the prototyping time and to conserve high processing performances for instance implementation based on:

- heterogeneous architectures [1] that mixed reconfigurable logic (i.e. FPGA) and embedded processor,
- high-level abstraction description and the associated fast prototyping tools [2][3][4],
- multi-core processor architectures such as Digital Signal Processors (DSP), Graphic Processor Units (GPU) or even Generic Purpose Processor (GPP).

In this paper, we propose to focus on implementation based on GPP due to the emergence of new generation of low-cost multi-core processors which enables high processing performances to be reached and therefore to match with some constraints of complex image-processing algorithms. The key idea of this development is to be able to propose fast prototyping using a low-cost smart camera based on this kind of target. Hence, we have developed a new framework dedicated to multi-core processor associated with an image sensor. The framework aims to offer a high degree of flexibility for managing the tasks and the memory allocation. Hence, the framework enables the priority and the allocation of each task to be controlled. Each task (or binary) is independent in terms of execution nevertheless it can be linked and controlled using a higher hierarchy level binary. The image acquisition task can be completely independent from the other processing tasks. One processor's core can even be dedicated to the acquisition task to guarantee a constant input data-flow to the image processing tasks. The data exchange is defined in POSIX, each binary can be therefore coded differently (for instance in C or C++, or in another languages) and offer a relative Operating System (OS) compatibility. The memory management enables a sequence of images to be automatically stored and a simultaneous access to be granted for several processings. The framework includes an interface dedicated to the management of the tasks: the user can add or suppress a binary during the runtime, logs or processing results can be visualised for each task.

The resulting framework has been used with the low-cost multi-core processor Raspberry2 platform coupled with its specific camera (1080p@30fps). The proposed architecture offers a Quad-Core ARM Cortex-A7 900 MHz associated to a Dual-Core VideoCoreIV GPU which enables to perform 1080p video decoding. The 1 Go memory space is double that of the previous Raspberry product. Using Operating Systems (OS), the resulting platform enables the user to access a low-cost embedded computer. The low-cost smart camera associated to the proposed framework enables fast prototyping of complex image processing. We focus on the extraction and the exploitation of visual information for smart building management. For instance, the people tracking would be a very useful processing in order to increase the level of security or services in the building. The Building Information Modeling (BIM) [5] regroups all the data which are involved in the building life-cycle management [6]. This priori information could be used, for instance, to simplify the tracking process in a multi-view configuration.

Keywords—Smart Camera, Multi-core processor, Real-time Image processing, Development Framework, Shared Memory Management, Building Information Modeling (BIM)

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